



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

ml

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,050	01/29/2002	David R. Blythe	1026.00	3659

26111 7590 11/24/2006

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

LAY, MICHELLE K

ART UNIT PAPER NUMBER

2628

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/058,050

Applicant(s)

BLYTHE ET AL.

Examiner

Michelle K. Lay

Art Unit

2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 8-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9-14-06

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

The amendment filed 09/11/2006 has been entered and made of record. Claims 1-5 and 8-21 are pending.

Response to Arguments

Applicant's arguments with respect to claims 1-5 and 8-21 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendment.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/11/2006 is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1-5** and **8-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenworthy et al. (5,808,617).

In regards to claim 1, Kenworthy teaches a *method for minimizing an amount of data needed to test a geometry chunk in a frame against subarea boundaries in a compositing window, comprising the steps of:*

- ***defining the geometry chunk with a bounding region, wherein said bounding region defines a space the geometry chunk occupies on the compositing window;***

A scene, or portions of a scene, can be divided into pixel regions (e.g. 32x32 pixels), called chunks. The geometry is presorted into bins based on which chunk the geometry the geometry will be rendered into [col. 8, lines 32-39].

- ***storing said bounding region for use in processing the geometry chunk in a subsequent frame;***

Main memory (134) [Fig. 2].

- ***sending said bounding region to graphics pipelines;***

Gsprite chunk data is sent to the buffer [col. 12, lines 27-30].

Although not explicitly taught, it is implicit that the chunk boundary is communicated through the system via the memory control (136) that serves as an interface between the processor (132) and main memory (134) as shown in Fig. 2. The geometry is presorted into bins based on which chunk the geometry will be rendered into [col. 8, lines 32-39].

- ***determining a graphics pipeline of said graphics pipelines that will render the geometry chunk defined by said bounding region;***

The geometry is presorted into bins based on which chunk the geometry will be rendered into [col. 8, lines 32-39; col. 9, line 27].

- ***assigning a subarea in the compositing window to receive an output of said graphics pipeline; and***

A scene, or portions of a scene, can be divided into pixel regions, called chunks [col. 8, lines 32-39]. These regions

- ***communicating the geometry chunk to said graphics pipeline that will render the geometry chunk;***

The geometry is presorted into bins based on which chunk the geometry will be rendered into [col. 8, lines 32-39]. The image processor determines how the geometric primitives (e.g. polygons) should be divided among the chunks [col. 13, lines 55-60]. Although not explicitly taught, it is implicit that such information is communicated through the system via the system interface (110) as shown in Fig. 1.

- ***wherein said graphics pipelines are configured to render the frame by spatial compositing through parallel processing.***

The system of Kenworthy further teaches the use of double buffering, which enables the system to generate one display list while it reads another. As the system calculates the gsprite transforms and build the display list for one frame, it reads the display list for another frame and displays the image data in this list. Because of the double buffering, the image preprocessor performs steps (280-286) shown in Fig. 6, for one frame, which the image processor performs steps (290-298) for another frame [col. 15, lines 23-32].

In regards to claim **2**, the image processor determines how the geometric primitives (e.g. polygons) should be divided among the chunks [col. 13, lines 55-60].

In regards to claim **3**, Kenworthy teaches *wherein said space is a screen space* [col. 13, lines 50-54]. Additionally, as shown in Fig. 6, the images are read from shared memory (216), and transformed to physical output device coordinates (said *screen space*) by the gsprite engine (204) [col. 14, lines 25-31; col. 15, lines 44-45].

In regards to claim **4**, Kenworthy teaches *wherein said space is a world space* [com. 12, line 50].

In regards to claim **5**, Kenworthy teaches *wherein said space is an object space*.

The invention of Kenworthy transforms the bounding volume so that the number of chunks required to render the gsprite is minimized. Therefore, the space to which the objects assigned to the gsprite is not necessarily the screen space but referred to the gsprite space [col. 13, lines 47-54].

In regards to claim **8**, Kenworthy teaches a display list that defines which gsprites (i.e. chunks) are to be displayed on the screen [col. 14, lines 45-50].

In regards to claim 9, Kenworthy teaches geometry processing where each primitive has a series of vertices. The vertex includes position information. Although Kenworthy does not explicitly teach such vertices as the vertices associated with the chunk, the chunk consists of the primitives associated with the vertices and therefore, implicitly, the geometry chunk is represented as a vertex array object. Additionally, the system of Kenworthy consists of a vertex input processor (384), vertex and control registers (386) which is used for edge detections of the triangle [col. 17, lines 19-24].

In regards to claim 10, Kenworthy teaches the image preprocessor determines how the geometric primitives (e.g. polygons) should be divided among the chunks by transforms the polygons to 2-D space and determining which chunk or chunks the polygons project into. Due to the expense of clipping polygons, the preferred approach is to not clip the polygons lying at the edge of a chunk. Instead, a chunk includes polygons that overlap its edge. If a polygon extends over the border of two chunks, for example, the vertices of the polygon are included in each chunk. The image preprocessor then queues the chunk data for tiling. Tiling refers to the process of determining pixel values such as color and alpha for pixel locations covered or partially covered by one or more polygons [col. 13, line 55 – col. 14, line 2]. The tiler includes registers for six vertices to allow double buffering of the triangle processing [col. 17, lines 19-27].

In regards to claim **11**, claim 11 recites the same limitations as claim 1. Therefore, the same rationale used for claim 1 is applied. Furthermore, system of Kenworthy provides a graphics-rendering pipeline [*Abstract*]. The graphics support software (160) includes functions to support chunking and gsprite allocation (said **geometry distributor**) [col. 11, lines 21-40]. The graphics support software (160) executes on the host computer system (130) and communicates with the image processing board (164) through the hardware abstraction layer (162) (said **interface**) [col. 11, lines 14-20]. The image processor stores the compressed chunk in shared memory (262) [col. 15, lines 53-67]. Furthermore, the system of Kenworthy further teaches the use of double buffering, which enables the system to generate one display list while it reads another. As the system calculates the gsprite transforms and build the display list for one frame, it reads the display list for another frame and displays the image data in this list. Because of the double buffering, the image preprocessor performs steps (280-286) shown in Fig. 6, for one frame, which the image processor performs steps (290-298) for another frame (said **parallel processing**) [col. 15, lines 23-32].

In regards to claim **12**, the system of Kenworthy comprises a main memory (134) as illustrated in Fig. 2, that stores (134) programs comprising a series of instructions stored on a computer-readable medium [col. 10, lines 10-25]. As shown in Fig. 3, the block diagram illustrates the relationship between the software and hardware, where the image processing system is implemented using processing resources of the processor of the host computer and the image processing hardware [col. 11, lines 3-14].

In regards to claim **13**, as shown in Fig. 3 of the block diagram showing the relationship between hardware and software, the graphics support software (160) executes on the host computer system (130) and communicates with the image processing board (164) through the hardware abstraction layer (162) (said **interface**) [col. 11, lines 3-14].

In regards to claim **14**, the graphics support software (160) includes functions to support chunking and gsprite allocation [col. 11, lines 21-40]. Therefore, although not explicitly taught, it is implicitly that this information provided from the graphics software is then communicated to the image processing board (164) via the hardware abstraction layer (162).

In regards to claim **15**, claim 15 recites the same limitations as claim 3. Therefore, the same rationale used for claim 3 is applied.

In regards to claim **16**, claim 16 recites the same limitations as claim 4. Therefore, the same rationale used for claim 4 is applied.

In regards to claim **17**, claim 17 recites the same limitations as claim 5. Therefore, the same rationale used for claim 5 is applied.

Art Unit: 2628

In regards to claim **18**, Kenworthy does not explicitly disclose a bounding region calculator, however, the graphics support software (160) includes functions to support chunking and gsprite allocation, which therefore determines the bounding region for the geometry chunk [col. 11, lines 21-40]. Additionally, the system of Kenworthy presorts the geometry into bins based on which chunk the geometry will be rendered into [col. 8, lines 32-39], where each bin is the pipeline.

In regards to claim **19**, claim 19 recites the same limitations as claim 8. Therefore, the same rationale used for claim 8 is applied.

In regards to claim **20**, claim 20 recites the same limitations as claim 9. Therefore, the same rationale used for claim 9 is applied.

In regards to claim **21**, claim 21 recites the same limitations as claim 10. Therefore, the same rationale used for claim 10 is applied.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rentschler et al. (5,821,950)

Rentschler et al. (5,969,726)

Rentschler et al. (5,940,086)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

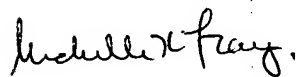
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday-Friday 7:30a-5p.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee M. Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

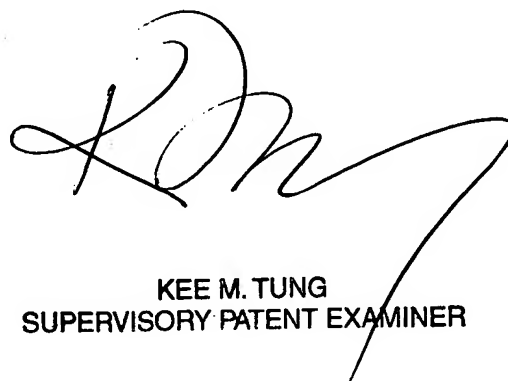
Art Unit: 2628

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michelle K. Lay
Patent Examiner
Division 2628
11.16.2006 mkl



PATENT EXAMINER



KEE M. TUNG
SUPERVISORY PATENT EXAMINER